

PARSEC'S FPGA PLATFORM FOR DEMONSTRATION AND TRAINING

1 TECHNICAL DESCRIPTION

This section provides more detail on the platform and the demonstration application to be used for training purposes.

1.1 FUNCTIONAL OVERVIEW

A functional diagram of the demonstration platform is shown in **Figure 1**.

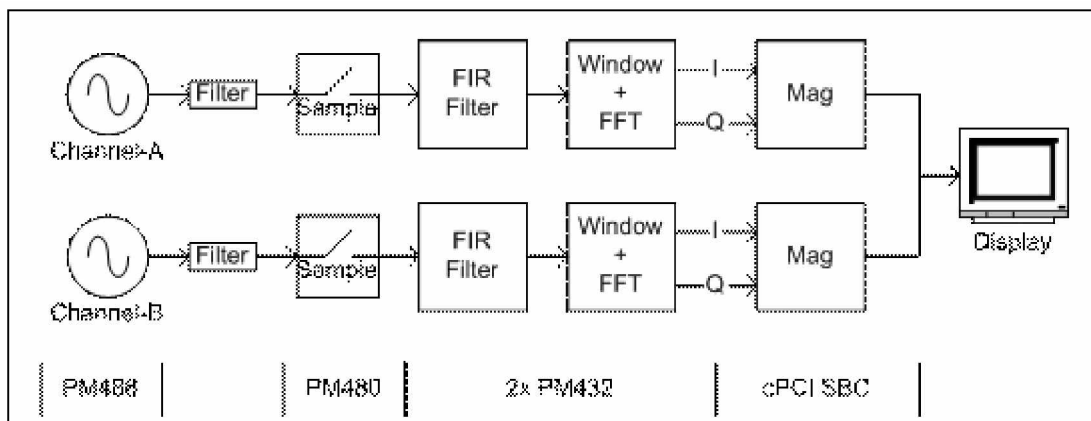


Figure 1: Demonstration platform functional diagram

The Compact PCI Single Board Computer (SBC) downloads two waveforms to the PM488 waveform buffers, from where they are simultaneously and continuously read out and converted into analogue signals. The two PM488 analogue outputs are connected to the PM480 analogue inputs via two low pass filters.

The PM480 captures 1K samples on each channel when it receives a software trigger. The captured samples of the two channels are transferred to the SBC via DMA. The SBC displays the sampled data of the two channels and then sends the data to the two PM432s for further processing. Both the PM480 and PM488 respectively use their 105MHz on-board oscillators for sampling and signal generation.

On the PM432s, the Processing FPGAs each receive the 1K samples from its associated PM480 analogue input via the SBC. FIR filtering is performed on the received data, after which the result is routed to the FFT block. FFT processing includes a programmable window function and a block floating-point FFT. After FFT processing the complex FFT results are sent to the SBC via DMA.

The demonstration application (Matlab .m file) runs on the SBC and generates a software trigger on the PM480. After sampled analogue data is received by the SBC, it is displayed and sent to the PM432s for processing. After the SBC receives the

complex FFT results from the PM432s, the magnitude is calculated and displayed for the two channels. The demonstration application then generates the next PM480 software trigger. This process runs continuously.

1.2 SPECIFICATIONS

A block diagram of the demonstration platform with the various cPCI and PMC components is shown in **Figure 2** below.

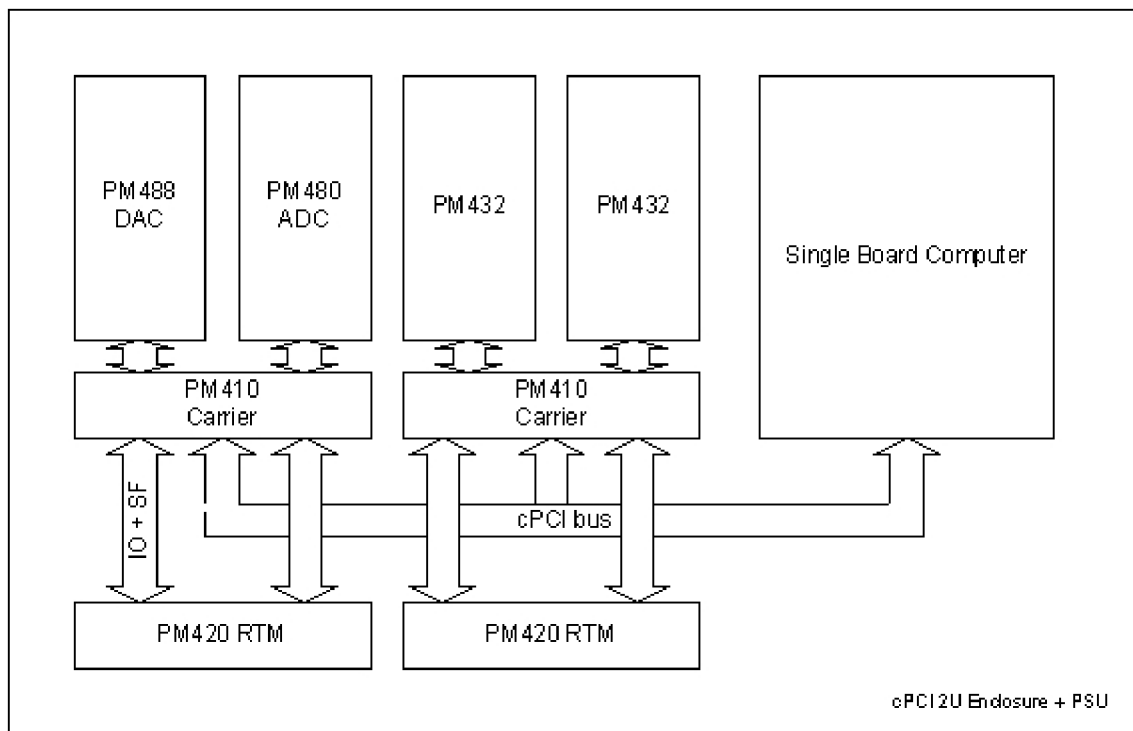


Figure 2. Demonstration platform block diagram

The High level specifications for each of the components shown above are:

1. PM488 dual channel 14-bit 150MSPS DAC PMC
 - Signal generation fixed at 105MSPS from on-board oscillator
2. PM480 dual channel 14-bit 105MSPS ADC PMC
 - ADC clock fixed at 105MSPS from on-board oscillator
 - Programmable sample rate of $105\text{MSPS} \div (1 \text{ to } 2048)$
 - Same trigger and sample rate for both channels
3. PM432 FPGA Processing PMC
 - 64-tap FIR filter with coefficients downloadable from SBC
 - Window function downloadable from SBC (default Blackman)
 - 1K block floating-point FFT

4. SBC
 - Pentium based board, with two PMC sites
 - 80GB or larger hard disk for SBC
 - Windows XP operating system
 - USB CD ROM DRIVE
5. Rack
 - 2U, Compact PCI 6U horizontal 4 slots, Pluggable PSU and integrated fans

Detailed brochures are available for Parsec products and can be supplied in PDF format on request.

1.3 TYPICAL APPLICATIONS

1. Spectrum and signal analyser.
2. Radar or other signal simulator.
3. Two channel non-coherent radar signal processor, for coherent radar the PM440 Clock and Trigger module (not included in this proposal) is also required.
4. Software defined radio.

Note that applications 2-4 require additional firmware and software to be developed on the demonstration platform.

1.4 TRAINING AND COMMISSIONING

As part of the delivery of the system, Parsec will facilitate a five day training session on the demonstration platform at a Parsec venue. During the training, the customer will learn to use the demonstration platform and to access and modify the firmware reference design. The specifications listed in this quotation will be verified during the training session.

The pace of training will be adjusted to ensure that trainees fully understand the covered concepts before moving to the next topic, therefore all workshops might not be completed during the training.

The training only includes Matlab software and excludes any C based software.

Parsec based the agenda on the following assumptions which would require verification before training commences:

1. The members attending the training are proficient with VHDL as design language
2. Team members will be available for a 5 day training course
3. Team members will have notebooks loaded with the correct Software

The preliminary agenda for the training is as follows:

Day	Session	Topics covered
1	Introduction	Provide an overview of the VHDL language and Altera FPGA technology. - Theoretical training
2	Tool Set and COTS overview	<u>Work through the tool flow required to do design work on the Demo Platform:</u> - Mentor Graphics HDL Designer version 2002.1b - Mentor Graphics Modelsim PE version 5.6a - Altera Quartus II version 7.0 and accompanying IP cores (FIR and FFT) - Altera FIR Compiler - Altera FFT Core - Matlab Release 14 or later <u>COTS overview:</u> - Overview of COTS modules
3	Reference firmware simulation and test	<u>Workshop #1: Compile, simulate and test Reference firmware:</u> - Overview of the HW, SW and Firmware components in the Demo Platform - Theory of DSP building blocks used in the System - Compile the Reference firmware and simulate - Test on the Demo Platform
4	Reference firmware & software update, simulation and test	Workshop #2: Change Reference firmware and software, simulate and test on the Demo Platform
5	Advanced design changes	Workshop #3: Advance change to Reference firmware and software. Training wrap-up and final questions